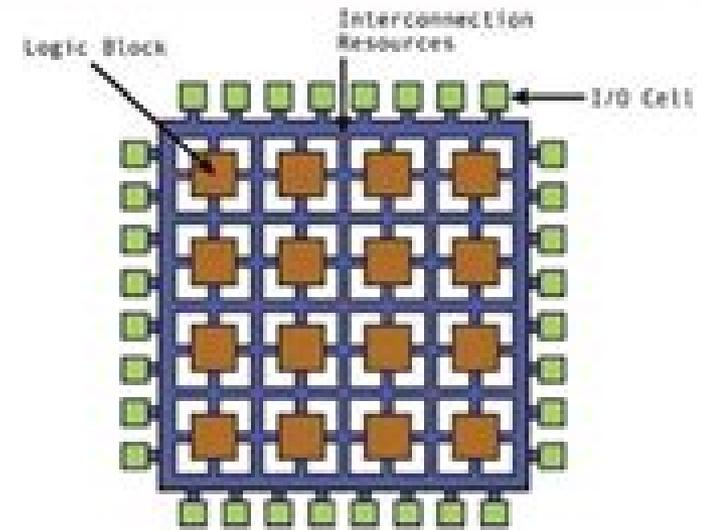


# Gate arrays

- The transistors level masks are fully defined and the designer can not change them.
- Program the wiring and vias to implement the desired function.
- We take a die which have all gates placed but not connected.
- Only layout of interconnect is given to fabrication house.



- Gate array designs are slower than cell-based designs but the implementation time is faster as less time must be spent.
- RTL-based methods and synthesis, together with other CAD tools, are often used for gate arrays.
- Efficiency decreases with GA

# Design Of Vlsi Gate Array Ics

**N Colangelo**



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