



An Architecture for Combinator Graph Reduction



Philip John Koopman, Jr.

An Architecture For Combinator Graph Reduction

Malcolm J. Shute



An Architecture For Combinator Graph Reduction:

An Architecture for Combinator Graph Reduction Philip John Koopman, 2014-05-12 An Architecture for Combinator Graph Reduction examines existing methods of evaluating lazy functional programs using combinator reduction techniques implementation and characterization of a means for accomplishing graph reduction on uniprocessors and analysis of the potential for special purpose hardware implementations Comprised of eight chapters the book begins by providing a background on functional programming languages and existing implementation technology Subsequent chapters discuss the TIGRE Threaded Interpretive Graph Reduction Engine methodology for implementing combinator graph reduction the TIGRE abstract machine which is used to implement the graph reduction methodology the results of performance measurements of TIGRE on a variety of platforms architectural metrics for TIGRE executing on the MIPS R2000 processor and the potential for special purpose hardware to yield further speed improvements The final chapter summarizes the results of the research and suggests areas for further investigation Computer engineers programmers and computer scientists will find the book interesting

An architecture for combinator graph reduction Philip John Koopman (Jr), 1989 Graph Reduction Joseph H. Fasel, 1987-10-07 This volume describes recent research in graph reduction and related areas of functional and logic programming as reported at a workshop in 1986 The papers are based on the presentations and because the final versions were prepared after the workshop they reflect some of the discussions as well Some benefits of graph reduction can be found in these papers A mathematically elegant denotational semantics Lazy evaluation which avoids recomputation and makes programming with infinite data structures such as streams possible A natural tasking model for fine to medium grain parallelism The major topics covered are computational models for graph reduction implementation of graph reduction on conventional architectures specialized graph reduction architectures resource control issues such as control of reduction order and garbage collection performance modelling and simulation treatment of arrays and the relationship of graph reduction to logic programming

Proceedings of the 1995 International Conference on Parallel Processing Prithviraj Banerjee, 1995-08-08 This set of technical books contains all the information presented at the 1995 International Conference on Parallel Processing This conference held August 14 18 featured over 100 lectures from more than 300 contributors and included three panel sessions and three keynote addresses The international authorship includes experts from around the globe from Texas to Tokyo from Leiden to London Compiled by faculty at the University of Illinois and sponsored by Penn State University these Proceedings are a comprehensive look at all that's new in the field of parallel processing

Proceedings of the 1990 International Conference on Parallel Processing Benjamin W. Wah, David A. Padua, Pen-Chung Yew, Pennsylvania State University, 1990 The field of parallel processing is maturing into a strong diverse and highly international area of study For the 1990 conference the eighteenth to be held over 500 papers were submitted by authors from 28 countries These three volumes make available the 256 papers that were accepted after a rigorous process of

review The overall variety and currency of issues addressed by the collection will make these volumes of vital interest to engineers scientists programmers systems analysts managers and other involved in the theory design and application of parallel processing

Combinator Graph Reduction David Lester,1989 As strictness analyses are usually used with confluent languages methods are discussed to restore this property The operational semantic model uses indirection nodes to implement sharing An alternative which is without indirection nodes is shown to be operationally equivalent for terminating programs The G machine is shown to be a representation of the combinator graph reduction operational model It may be represented by the composition of a small set of combinators which correspond to an abstract machine instruction set Using a modified form of graph isomorphism alternative sequences of instructions are shown to be isomorphic and hence may be used interchangeably

ACM Transactions on Programming Languages and Systems Association for Computing Machinery,1992 Contains articles on programming languages and their semantics programming systems storage allocations and garbage collection languages and methods for writing specifications testing and verification methods and algorithms specifically related to the implementation of language processors

An Effective Speculative Evaluation Technique for Parallel Supercombinator Graph Reduction James S. Mattson,1993

The Architecture of Symbolic Computers Peter M. Kogge,1991 Focuses on the design and implementation of two classes of non von Neumann computer architecture those designed for functional and logical language computing

S-K Reduction Engine for an Applicative Language Thomas Sear Clark,1982

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12th IMACS World Congress, July 18-22, 1988, Paris, France Robert Vichnevetsky,Pierre Borne,J. Vignes,1988

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